

Code No: P21ECT04

HALL TICKET NUMBER

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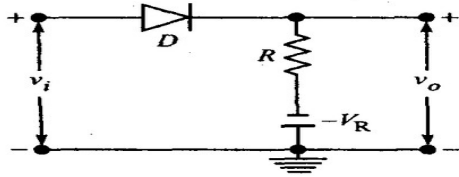
PACE INSTITUTE OF TECHNOLOGY & SCIENCES::ONGOLE
(AUTONOMOUS)

II B.TECH I SEMESTER END REGULAR EXAMINATIONS, JAN - 2023
PULSE AND DIGITAL CIRCUITS
(ECE Branch)

Time: 3 hours

Max. Marks: 70

Answer all the questions from each UNIT (5X14=70M)

Q.No.	Questions	Marks	CO	KL
UNIT-I				
1.	a) Derive the response of RC low-Pass Circuit excited by Step input signal	[7M]	1	3
	b) A 10 Hz square wave is fed to an amplifier. Calculate and plot the output waveform under the following conditions. The lower 3 dB frequency is: (a)3 Hz (b)30 Hz	[7M]	1	3
OR				
2.	a) Derive the response of RC high-Pass Circuit excited by ramp input signal	[7M]	1	3
	b) Justify that a high pass RC circuit act as a differentiator	[7M]	1	2
UNIT-II				
3.	a) Analyze the operation of Shunt diode clippers with circuits	[7M]	2	3
	b) Draw the output characteristics of the circuit shown below. Assume the diode is Ideal. 	[7M]	2	3
OR				
4.	a) A 100 V peak square wave with a period of 20 ms, is to be positively clamped at 25 V. Draw the circuit diagram necessary for this purpose. Draw the output waveform.	[7M]	2	3
	b) State and prove clamping circuit theorem	[7M]	2	3
UNIT-III				
5.	A fixed biased binary uses npn silicon transistors with $V_{CE(sat)}=0.5V$, $V_{BE(sat)}=1V$, $V_{BE(cutoff)}=0V$ and circuit parameters are: $V_{CC}=V_{BB}=6V$, $R_C=1.2k\Omega$, $R_1=4.7k\Omega$, $R_2=27k\Omega$. Find $h_{FE(min)}$ and stable state currents and voltages.	[14M]	4	3
OR				
6.	a) Show that an astable multivibrator can be used as a voltage to frequency converter.	[7M]	4	3
	b) Describe the operation of bidirectional sampling gates using transistor.	[7M]	4	2
UNIT-IV				
7.	a) Obtain an expression for oscillating frequency of UJT sweep generator	[7M]	4	3
	b) In a UJT sweep circuit $R=100k\Omega$, $C=0.01\mu F$ and $\eta=0.8$ find the frequency of oscillations.	[7M]	4	3
OR				



8.	a)	Why the time base generators are called sweep circuits? Give most important applications of time –base generators.	[7M]	4	2
	b)	Discuss the operation of transistor miller time base circuit.	[7M]	4	2
UNIT-V					
9.	a)	Draw and explain the circuit diagram of integrated positive RTL NOR gate.	[7M]	5	2
	b)	What is the major difference between TTL and ECL? Why does the propagation delay occur in logic circuits?	[7M]	5	2
OR					
10.	a)	Explain the characteristics and implementation of the following digital logic family i) CMOS, ii) ECL	[7M]	5	2
	b)	Draw and explain the circuit diagram of in TTL NAND & NOR gates.	[7M]	5	2
